

1. Schematic Page Description :

Origins Schematic Ver :

01

SoC I2C table

Function	Channel	Read	Write
NA	I2C0	0x?	
PMIC	I2C1	0x?	0x?
Audio codec	I2C4		
Track Pad	I2C5		
EC	I2C6		

EC SMBus/I2C table

Function	Channel	Address
Battery/charger	SMB0	
NA	SMB1	
PCH	I2C1	
NA	I2C2	
Thermal	I2C3	

Current sensor address

Function	Channel	Function	Channel
+VBATA	0x47	+VCC_OUT	0x40
+V5A	0x43	+VGG	0x44
+V3P3A	0x4B	+VNN	0x45
+V1P05A	0x46	+VDDQ_OUT	0x41
+V1P8A	0x49		

USB3/2 port mapping

USB3 Port No#	Usage	USB2 Port No#	Usage
USB3P0	NA	USB2P0	NA
USB3P1	I/O	USB2P1	I/O(3.0)
USB3P2	I/O	USB2P2	I/O(3.0)
USB3P3	NA	USB2P3	CCD
		USB2P4	BT

PCIe port mapping

PCIe port No#	Usage	PCIe CLK#	Usage
PCIe_0	NA	PCIe_CLK0	NA
PCIe_1	NA	PCIe_CLK1	NA
PCIe_2	WLAN	PCIe_CLK2	WLAN
PCIe_3	NA	PCIe_CLK3	NA

The diagram illustrates the system architecture centered around the Intel Braswell processor. Key components and connections include:

- Processor:** Intel Braswell, Power: TDP 6 Watt, Package: FCBGA 1170, Size: 25 x 27 (mm).
- Memory:** LPDDR3 (Memory down 4Pcs, 2 Channel) connected via LPDDR3 interface.
- Storage:** eMMC 5.0 (16G/32G) connected via MMC; SD Card connected via SD Card 3.0.
- BIOS/ROM:** 1.8V BIOS+TXE SPI ROM (64Mb) W25Q64FWSSIG connected via SPI Interface.
- Connectivity:**
 - DDI 1 (X2 LANES) connected to LCD Conn.
 - DDI 2 connected to HDMI Conn.
 - I2C Interface connected to PMIC, Audio Codec (ALC5650), Track Pad, and KBC (MEC1322).
 - USB 3.0 Interface (Port0/3, Port2, Port1) connected to USB3.0 Port x 1, Charger (SN1408009RTER), and Daughter Board.
 - USB 2.0 Interface (Port0, Port4, Port3, Port1) connected to CCD and Daughter Board.
 - PCIE Gen 2 x 1 Lane connected to NGFF M.2 2230-E (USB port3, WLAN / BT Combo, PCIE CLK PORT 2).
 - LPC Interface connected to TPM (SLB9655TT1.2 FW4.32GOOG), KBC (MEC1322-LZY), and Battery.
- Other Components:**
 - TPM (SLB9655TT1.2 FW4.32GOOG).
 - KBC (MEC1322-LZY, Package: DQFN132, Size: 11 x 11 (mm)).
 - Battery connected via SMB0 and SMB3.
 - Thermal IC (TMP432).
 - Keyboard.
 - Audio Codec (REALTEK ALC5650, Package: QFN-48, Size: 6 x 6 (mm)).
 - Speaker.
 - Combo Jack (Headphone + MIC).
 - DMIC.
 - Charger (BQ24770 NVDC Battery Charger).
 - RT7291 (+V5A) and RT7290 (+V3P3A).
 - PMIC RT5067 (+VNN, +V1P05A, +V1P8A, +V1P8U, +V1P8S, +V3P3A PRIM, +V1P15S, +V1P24A, +VDDQ_VTT).
 - RT9610/CSD87381P (+VCC, +VGG, +VDDQ).
 - Thermal Protection Discharger.

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U17A



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BRASWELL - MEMORY LPDDR3 CHANNEL B

07

SoC (CPU)

BSW_MCP_EDS

U17B

?




BSW_MCP_EDS

REV=1

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?

		PROJECT : NL6D	
		Quanta Computer Inc.	
Size	Document Number	Rev 1A	
BSW 2/10 (DDR8)			
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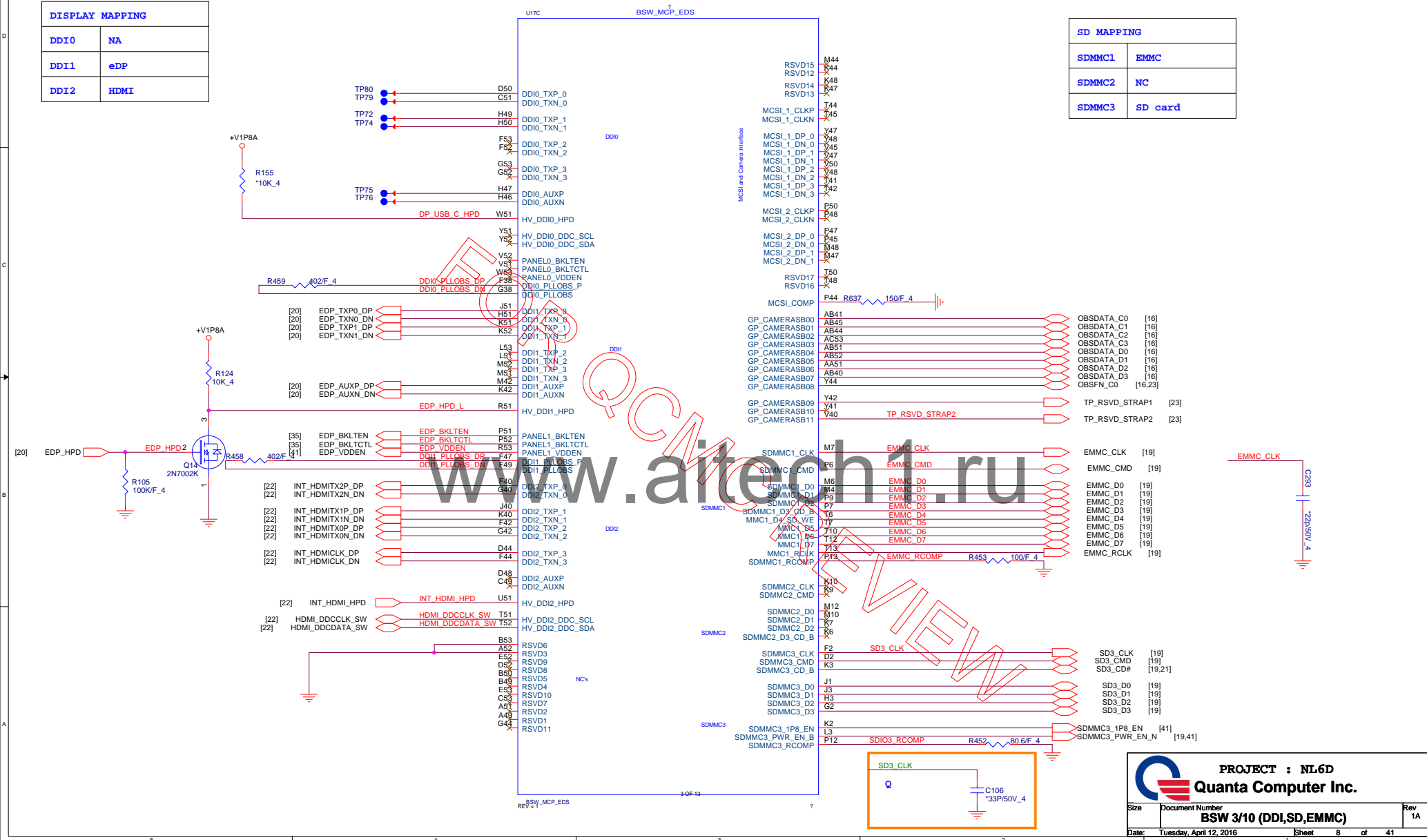
SoC (CPU)


DISPLAY MAPPING

DDI0	NA
DDI1	eDP
DDI2	HDMI

SD MAPPING

SDMMC1	EMMC
SDMMC2	NC
SDMMC3	SD card



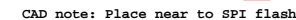
		PROJECT : NL6D Quanta Computer Inc.	
Size	Document Number	Rev	
	BSW 3/10 (DDI,SD,EMMC)	1A	
Date:	Tuesday, April 12, 2016	Sheet	8 of 41

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PCIe MAPPING	
PCIe0	NC
PCIe1	NC
PCIe2	WIFI (StP)
PCIe3	NC

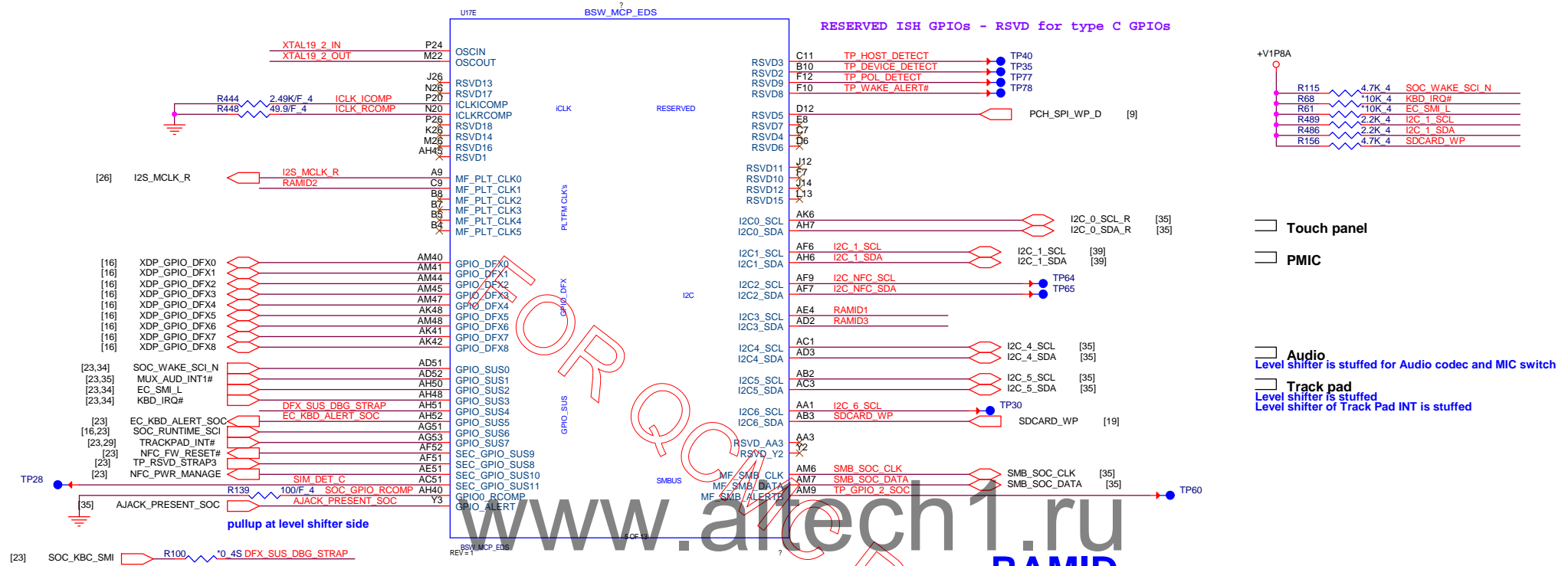


From debug header

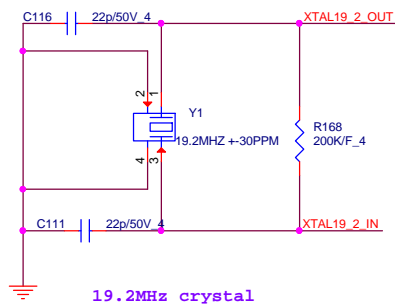
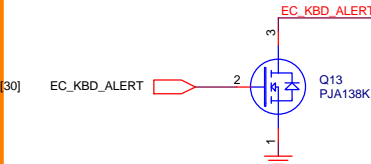


For ICT, place on TOP side

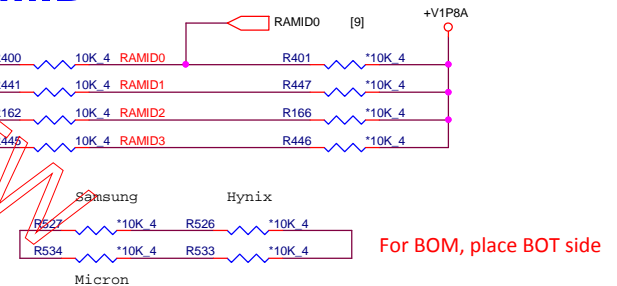
SoC (CPU) BRASWELL - I2C, XDP, SM BUS



19.2MHz X'tal

0312 added KBD_ALERT pin to notify SoC to lock ME FW
Keep reserving this feature in DVT build

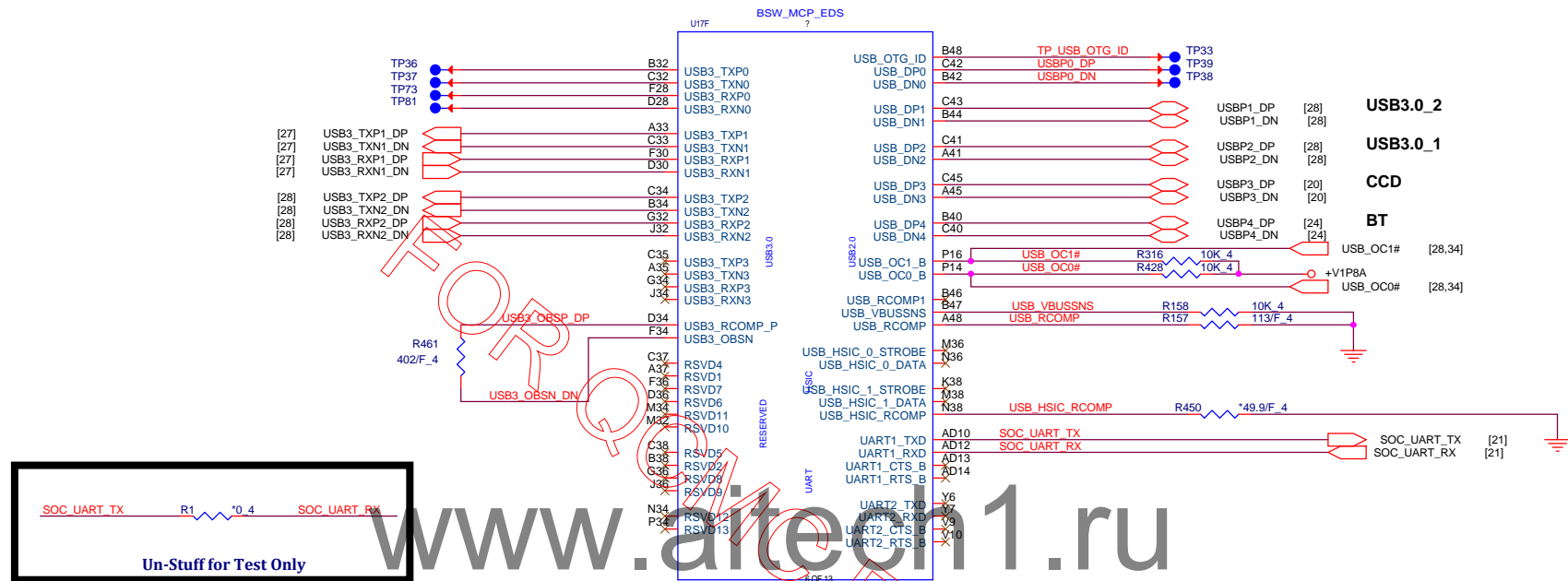
Vender	RAM_ID3	RAM_ID[2..0]	Q PN	Mfr. PN	Freq.	Size	Total Size
Samsung	0 (1-CH)	000	AKD5QWST508	K4E8E304EE-EGCF	1866MHz	4Gb	2Gb
Hynix	0 (1-CH)	001	AKD5RW0TW53	H9CCNN8GTMLAR-NUD	1866MHz	4Gb	2Gb
Micron	0 (1-CH)	010	AKD5QWSTL01	MT52L256M32D1PF-107	1866MHz	4Gb	2Gb
Samsung	0 (1-CH)	011	AKD5QWST521	K4E8E324EB-EGCF	1866MHz	4Gb	2Gb
Micron	0 (1-CH)	100	AKD5QWWT401	EDF8132A3MA-JD-F-R	1866MHz	4Gb	2Gb
Samsung	1 (2-CH)	000	AKD5QWST508	K4E8E304EE-EGCF	1866MHz	4Gb	4Gb
Hynix	1 (2-CH)	001	AKD5RW0TW53	H9CCNN8GTMLAR-NUD	1866MHz	4Gb	4Gb
Micron	1 (2-CH)	010	AKD5QWSTL01	MT52L256M32D1PF-107	1866MHz	4Gb	4Gb
Samsung	1 (2-CH)	011	AKD5QWST521	K4E8E324EB-EGCF	1866MHz	4Gb	4Gb
Micron	1 (2-CH)	100	AKD5QWWT401	EDF8132A3MA-JD-F-R	1866MHz	4Gb	4Gb



BRASWELL - USB INTERFACE

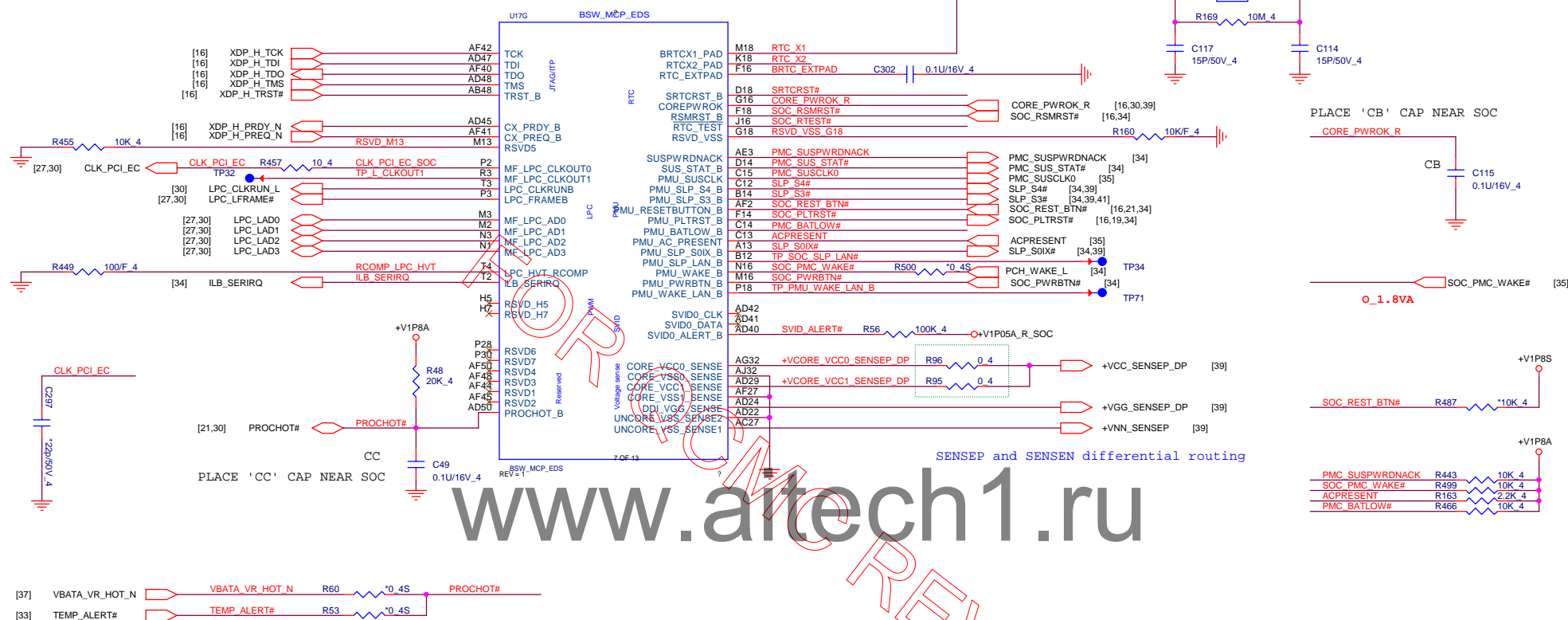
11

SoC (CPU)

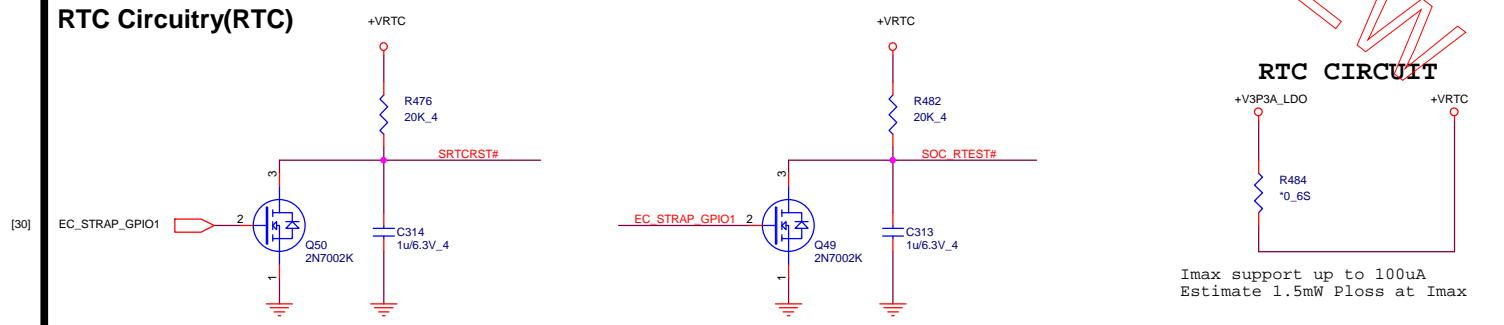


BRASWELL - JTAG, LPC, THERMAL, PMU

SoC (CPU)



RTC Circuitry(RTC)



Imax support up to 100uA
Estimate 1.5mW Ploss at Imax

PLACE THESE CAPS CLOSE TO
AA18, AA19, AA21, AA22, AA24, AA25,
AC18, AC19, AC21, AC22, AC24, AC25,
AD25 AND AD27

PLACE THESE CAPS CLOSE TO
V33, AA32, AA33, AA35, AA36,
AC32, Y30, Y32, Y33 AND Y35

PLACE THIS CAP CLOSE TO V19 AND V18

PLACE THESE CAPS CLOSE TO
AM21, AM33, AM22, AN22, AN32
AND AM32


PLACE THESE CAPS CLOSE TO
V22, V24, U24, U22, V27 AND U27

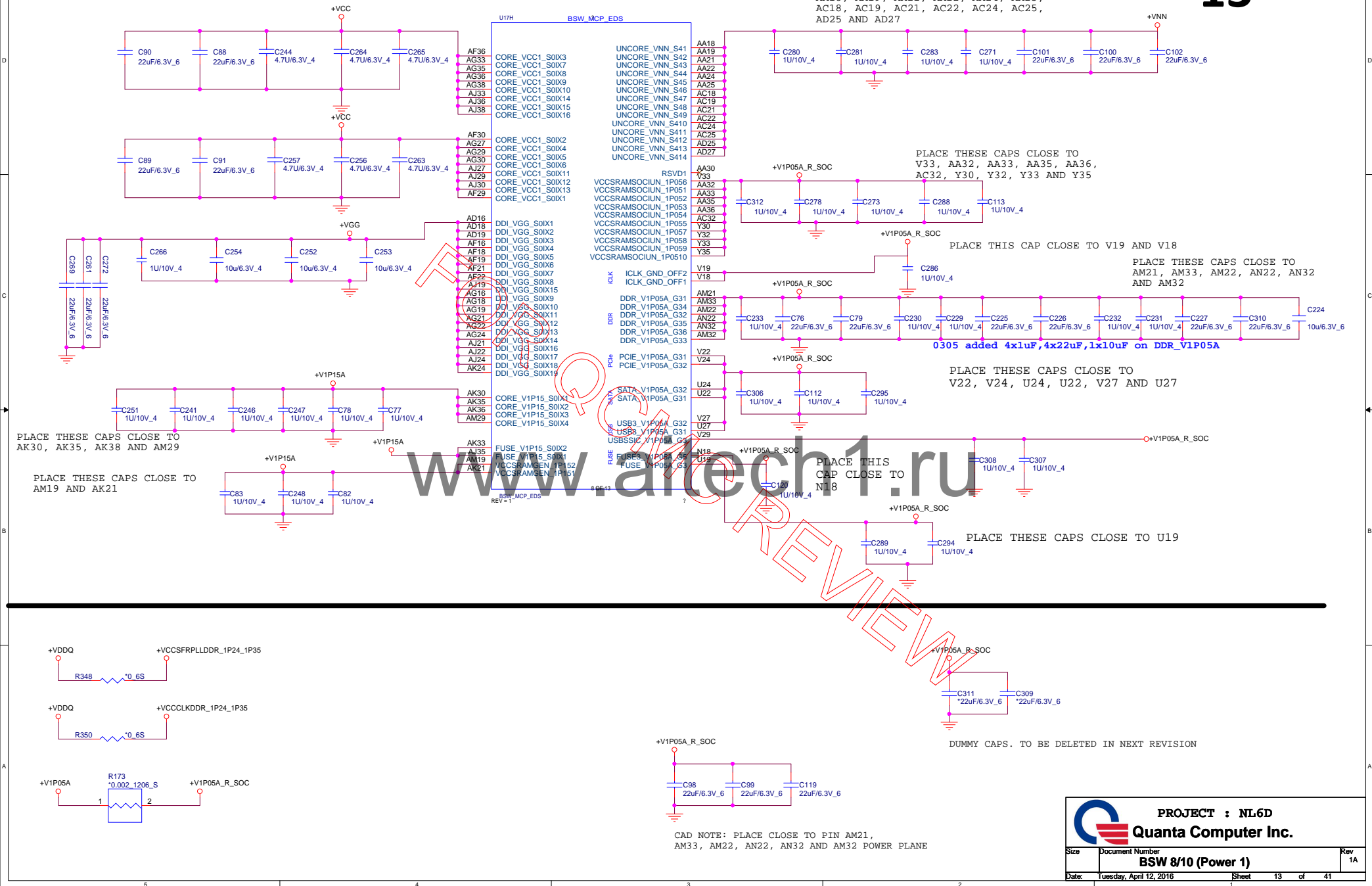
PLACE THIS
CAP CLOSE TO
N18

PLACE THESE CAPS CLOSE TO U19

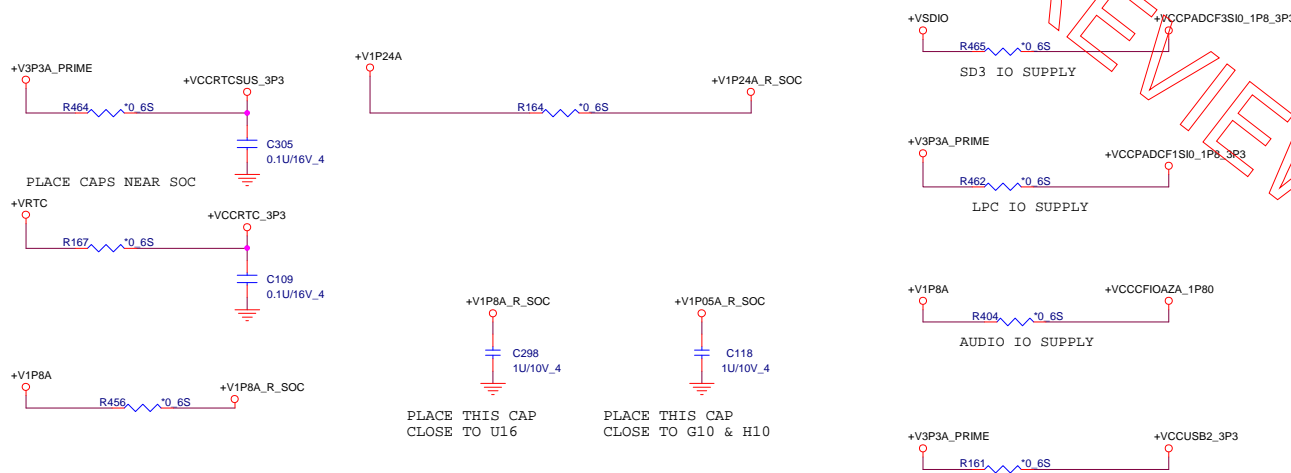
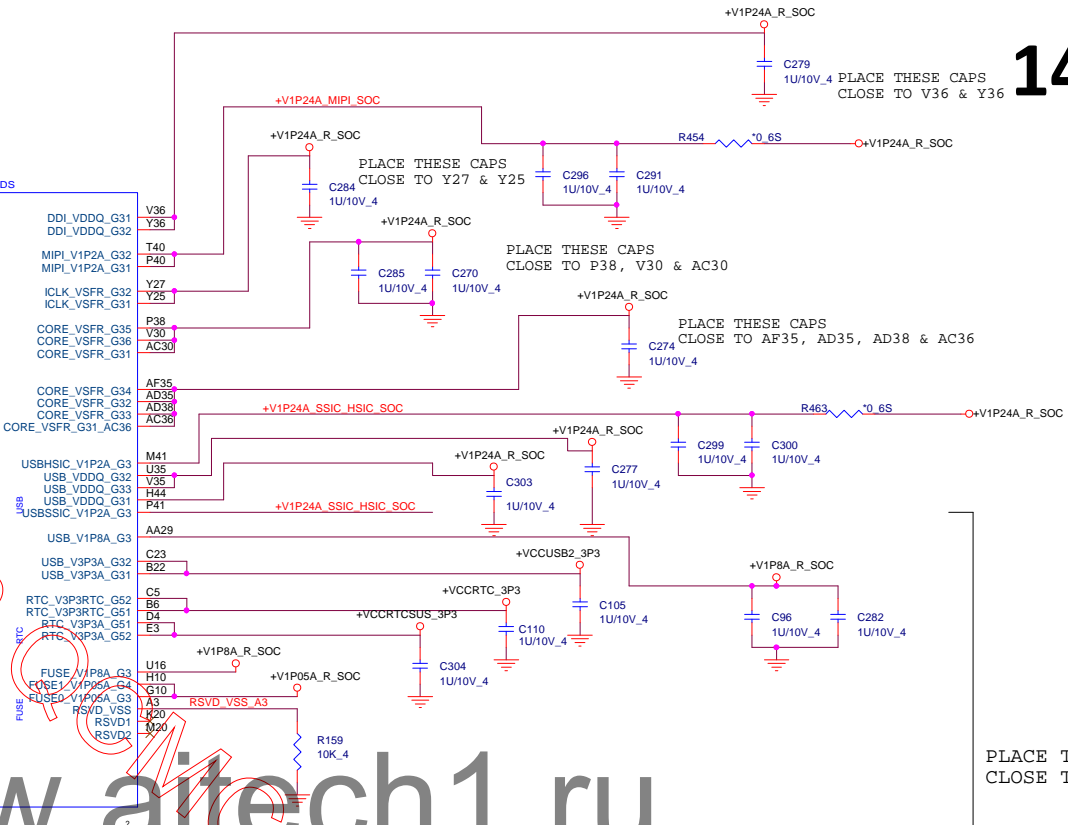
DUMMY CAPS. TO BE DELETED IN NEXT REVISION

CAD NOTE: PLACE CLOSE TO PIN AM21,
AM33, AM22, AN22, AN32 AND AM32 POWER PLANE

 PROJECT : NL6D Quanta Computer Inc.		
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	BSW 8/10 (Power 1)	1A
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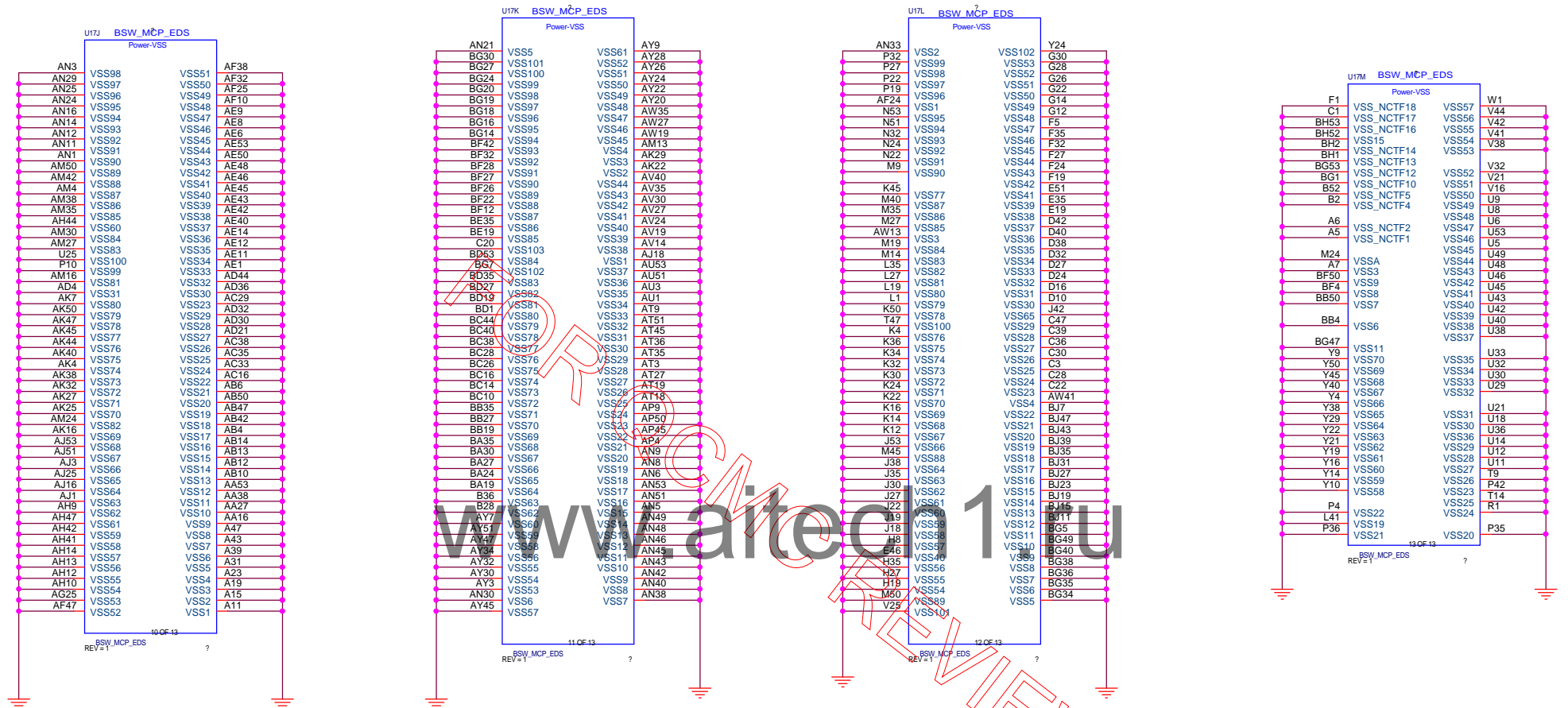


PLACE THESE CAPS
CLOSE TO THEIR PINS



BRASWELL - GND

15



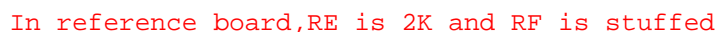
XDP (DBG)

16



APS

FOR XDP SIGNALS

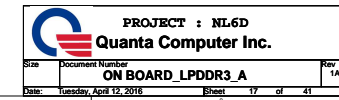


Size	Document Number XDP	Rev 1A
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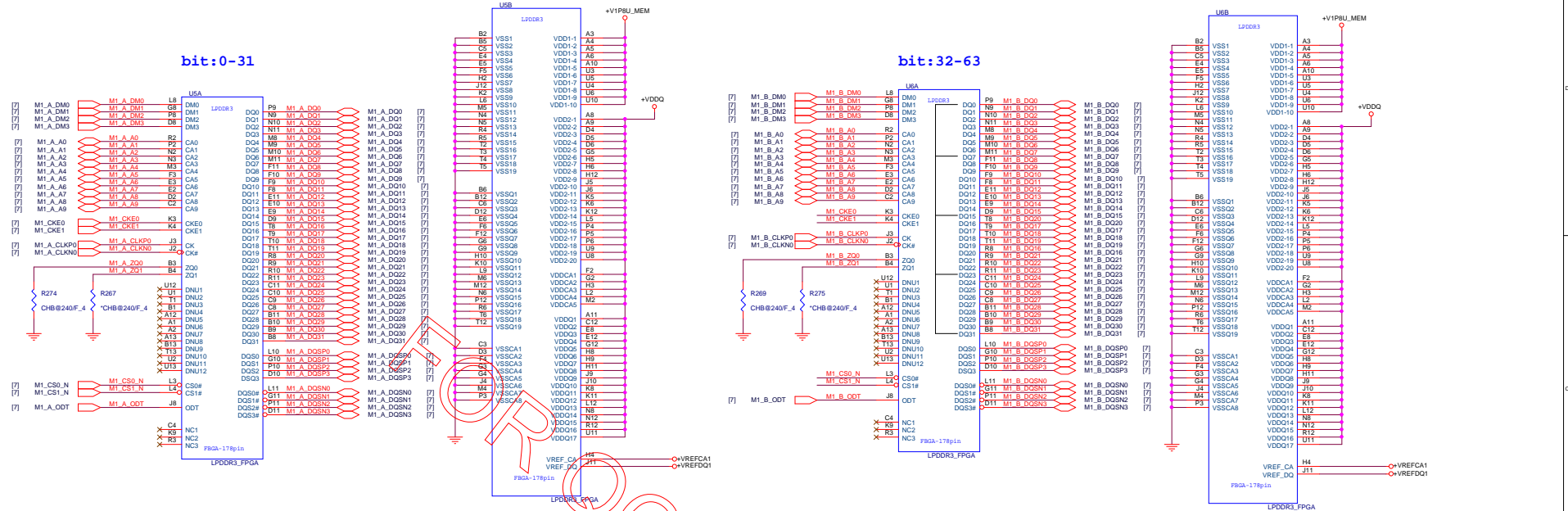
bit:32-63



VTT TERMINATIONS



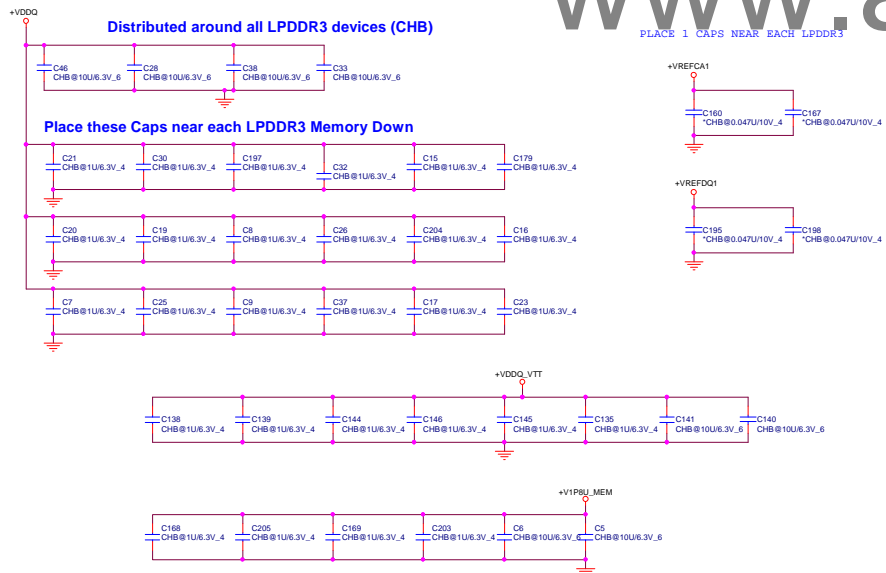
bit:32-63



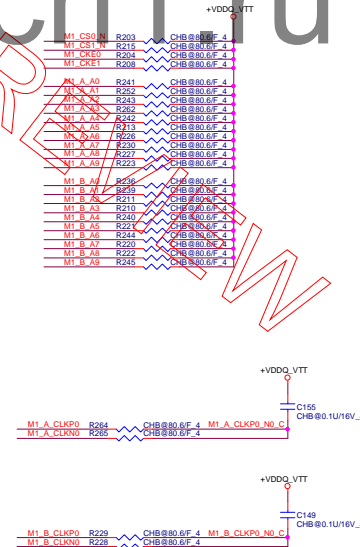
DE-CAPS FOR MEMORY CHANNEL B

Distributed around all LPDDR3 devices (CHB)

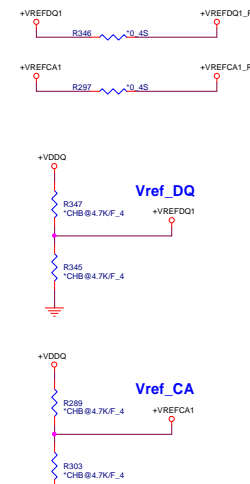
PLACE 1 CAPS NEAR EACH LPDDR3



VTT TERMINATIONS



VREF_DQ CIRCUIT



SD SLOT POWER SUPPLY

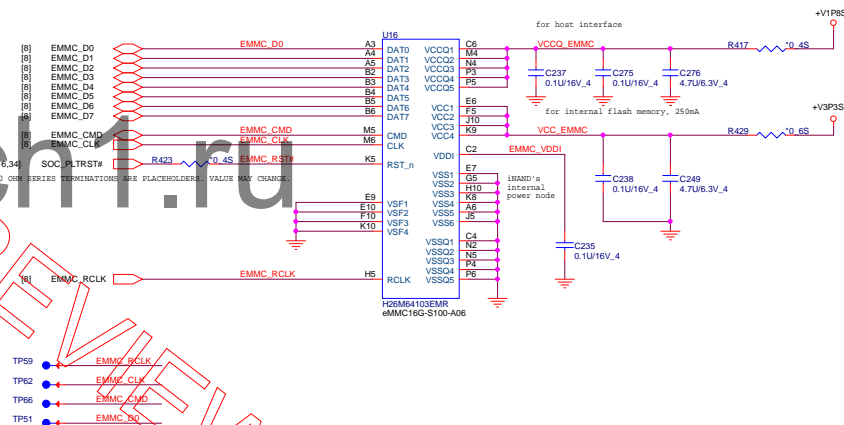


SD SLOT/EMI

This is full size SD card (push-push type)



eMMC



```

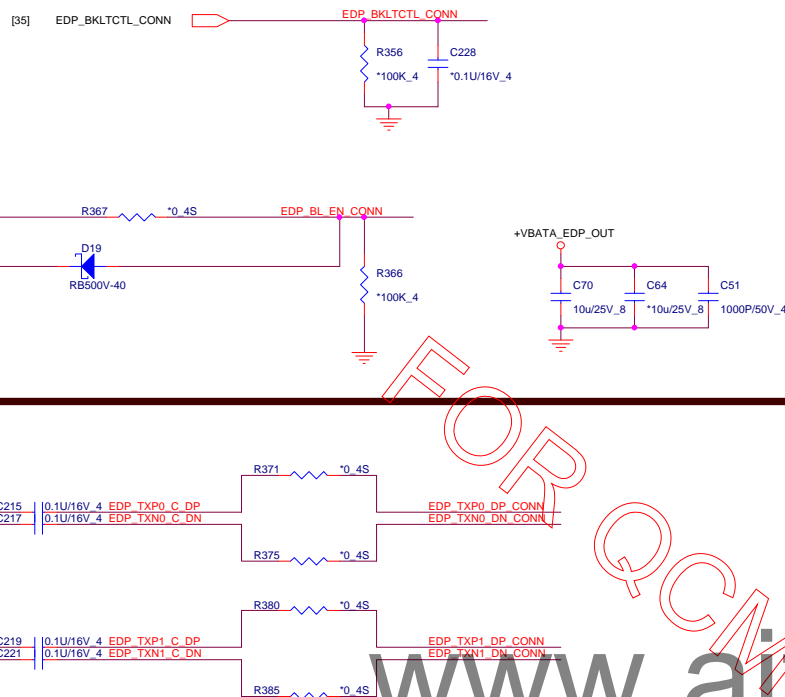
16G
Samsung-->KLMAG2WEMB-B031-AKE2RF-T505-- IC FLASH(153)KLMAG2WEMB-B031(FBGA)STNBSQ
Hynix--> H26M52103FMR (0x03)--AR0ZHQRI000--PROG IC FLASH(153P)H26M52103FMR STNBSQ

32G
Samsung-->KLMBQ4WECB-B031-AKE3S2-T500--IC FLASH(153)KLMBQ4WECB-B031(FBGA)STNBSQ
Hynix--> H26M641032MR (0x03)--AR0ZHQRI001--PROG IC FLASH(153P)H26M641032MR STNBSQ

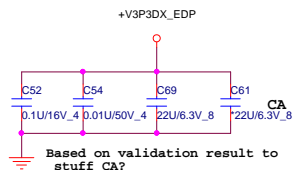
```

eDP PANEL CONTROL

LCD(LDS)

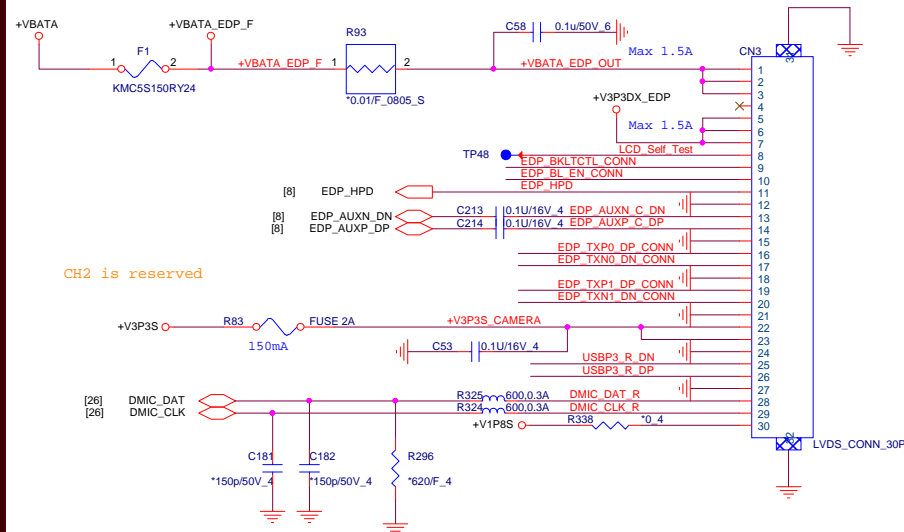


eDP Power



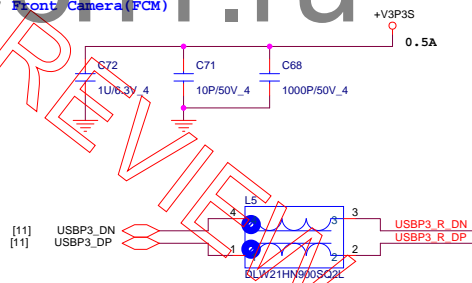
eDP CONNECTOR

LCD(LDS)

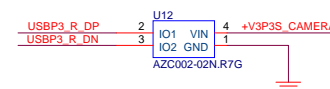


CAMERA - POWER AND USB CMC


Front Camera (FCM)



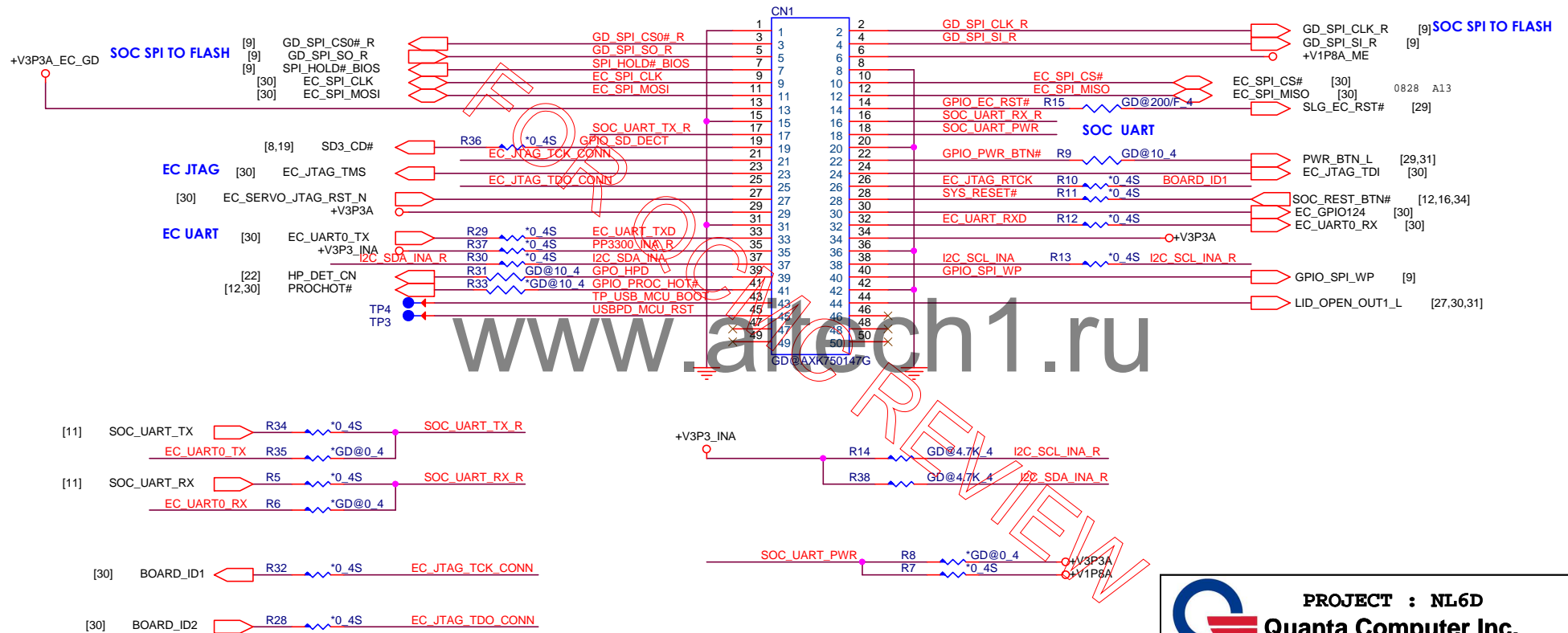
ESD



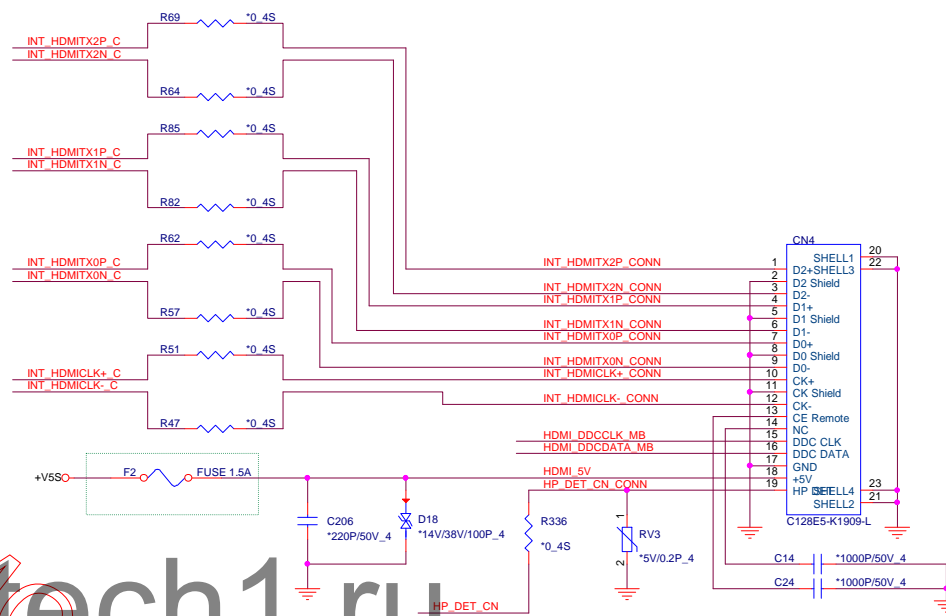
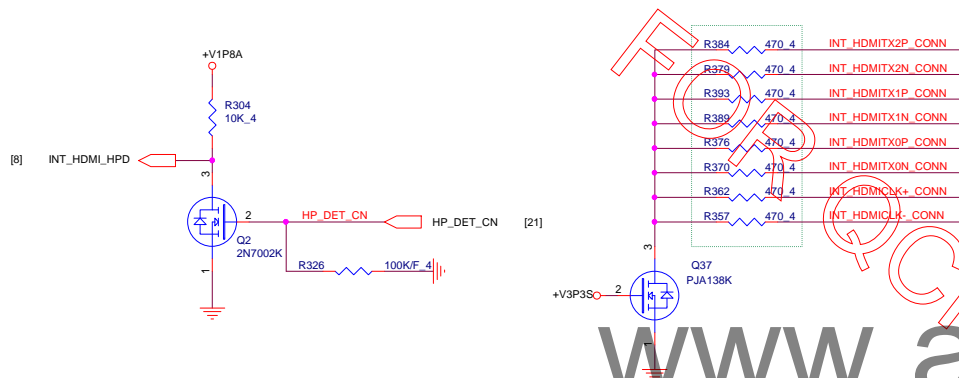
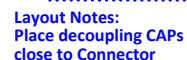
Layout note: Place close to CN9

		PROJECT : NL6D		Rev 1A
		Quanta Computer Inc.		
Size	Document Number eDP/CCD/DMIC			
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PIN7 OD	PIN39 OD	PIN49 OD
PIN14 OD	PIN41 OD	PIN50 OD
PIN19 OD	PIN43 OD	
PIN22 OD	PIN44 OD	
PIN28 OD	PIN45 OD	
PIN30 OD	PIN46 OD	
PIN37 OD	PIN47 OD	
PIN38 OD	PIN48 OD	

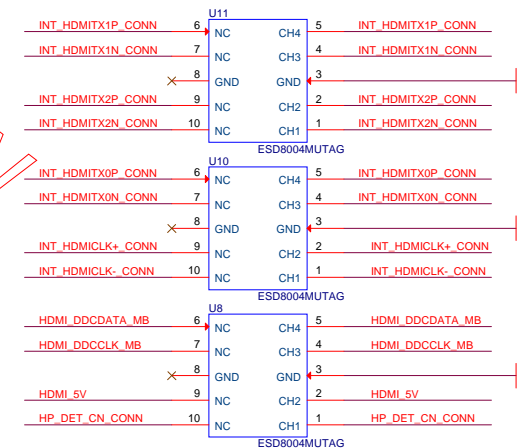
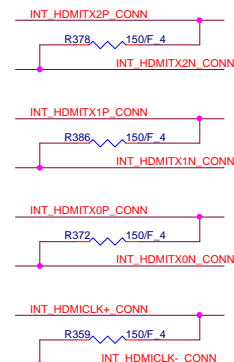


HDMI CONNECTOR



ESD 靠近HDMI CONNECTOR(CN2)

EMI

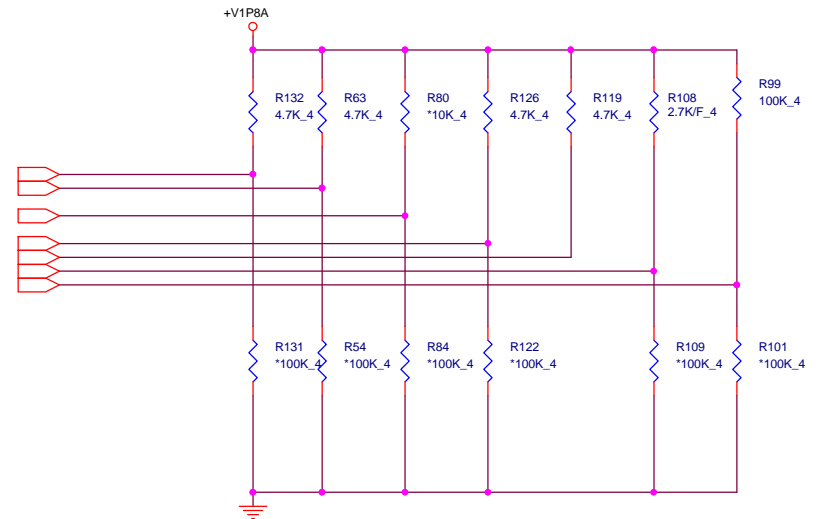


Layout note:Place close to HDMI Conn

BSW Strapping Table (based on EDS V1.0), sampled on the rising edge of PMU_RSMRST_N

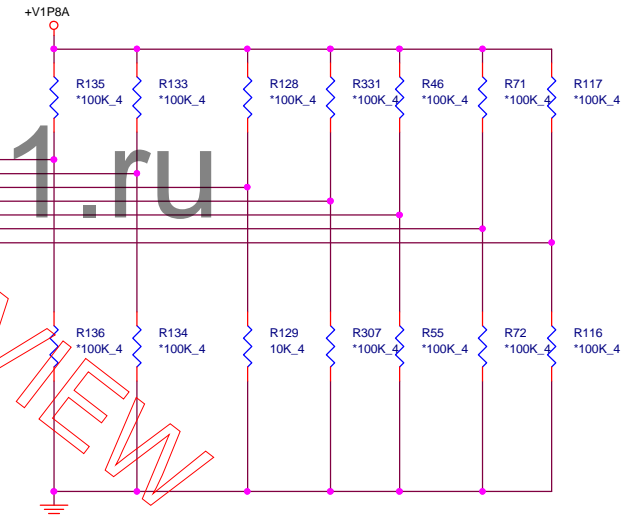
Pin Name	Strap description	Configuration
GPIO_SUS0	DDI0 Detect	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS1	DDI1 Detect	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS2	Top Swap (A16 Override)	0 = change boot loader address 1 = Normal operation
GPIO_SUS3	DSI Display Detect (Leave floating if GPIO functionality is not used, it is not POR)	0 = DSI not detected 1 = DSI detected
GPIO_SUS4	BIOS Boot Selection	0 = No SPI 1 = SPI
GPIO_SUS5	Security Flash Descriptors	0 = Not support 1 = Normal operation
GPIO_SUS6	Halt Boot strap	1 = Normal operation (MUST be high at RSMRST# de-assert to ensure proper platform operation and use of GPIO_DFX[8:0])
GPIO_SUS7	DFX SUS DEBUG strap	0 = SUSDUG 1 = No SUSDUG
GPIO_SUS8	PLLs, ICLK, USB2, DDI, SFR, supply select	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS9	ICLK, USB2, DDI, SFR Bypass	0 = No Bypass(Default) 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	0 = No Bypass(Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	0 = No Bypass(Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	0 = No Bypass(Default) 1 = Bypass

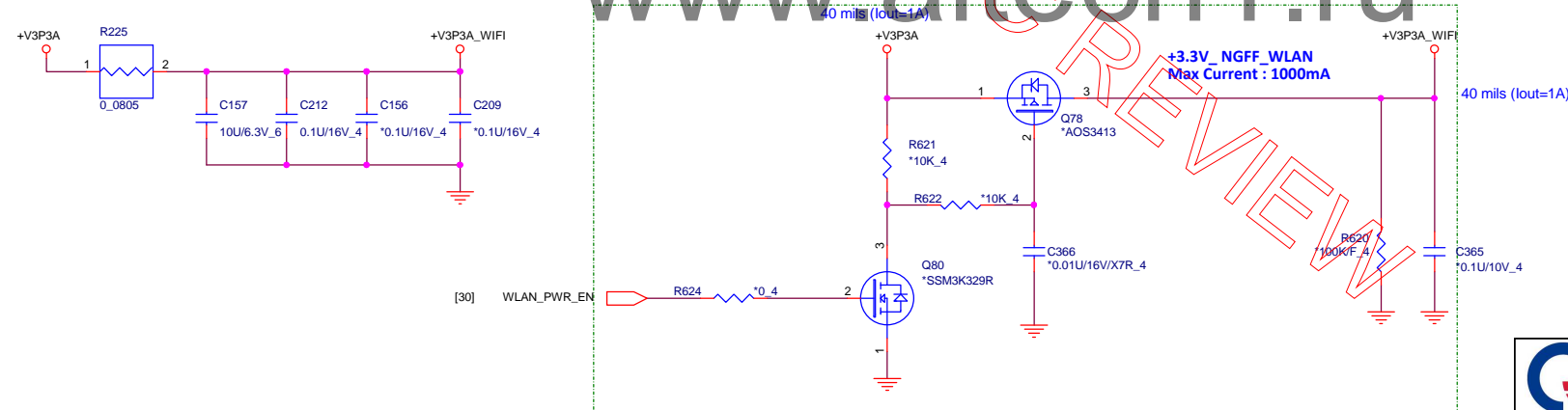
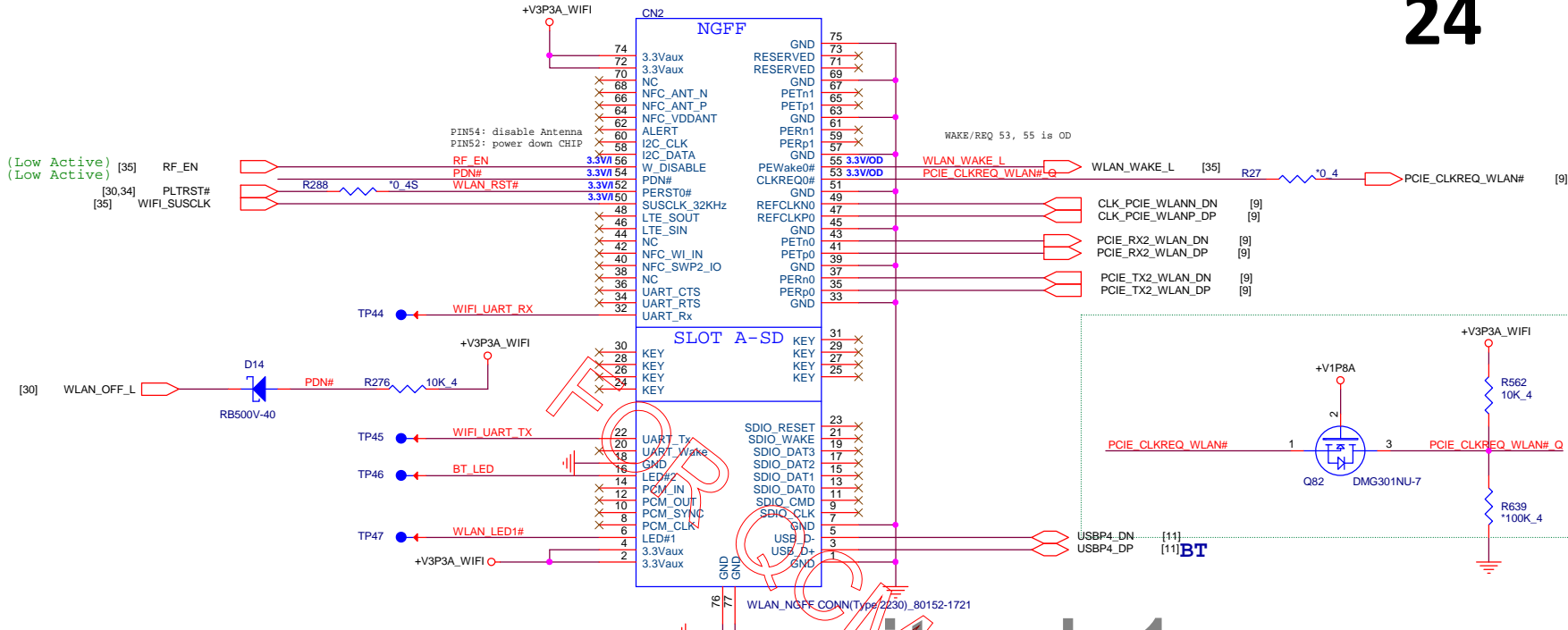
[10,35] MUX_AUD_INT1#
[10,34] EC_SMI_L
[10,34] KBD_IRQ#
[10,29] TRACKPAD_INT#
[10] EC_KBD_ALERT_SOC
[10,16] SOC_RUNTIME_SCI
[10] SOC_KBC_SMI



[10] NFC_PWR_MANAGE
[10] NFC_PW_RESET#
[10] TP_RSVD_STRAP3
[8,16] OBSFN_CO
[8] TP_RSVD_STRAP1
[8] TP_RSVD_STRAP2
[10,34] SOC_WAKE_SCI_N

NFC_PWR_MANAGE
NFC_PW_RESET#
TP_RSVD_STRAP3
OBSFN_CO
TP_RSVD_STRAP1
TP_RSVD_STRAP2
SOC_WAKE_SCI_N





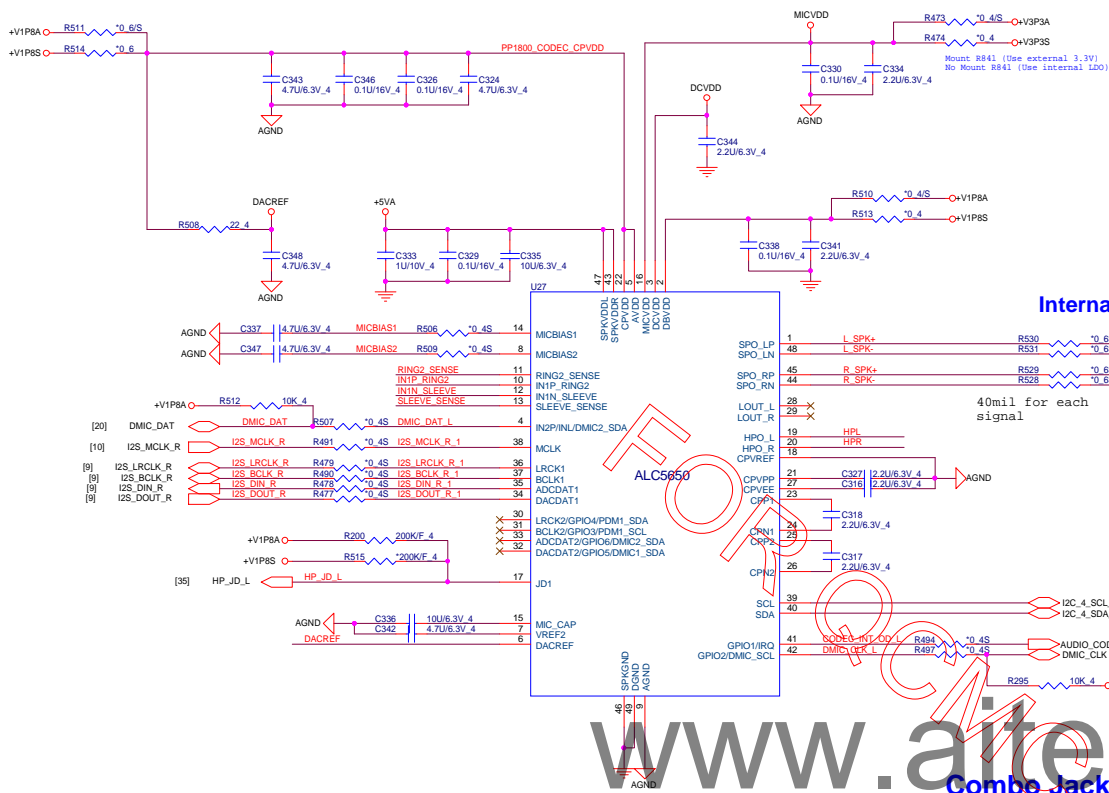
Removed (2015/03/27)

LTE NGFF (LTE)

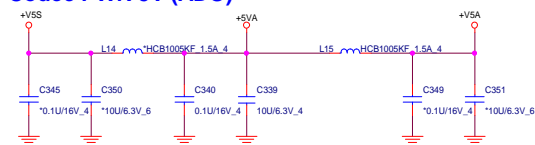
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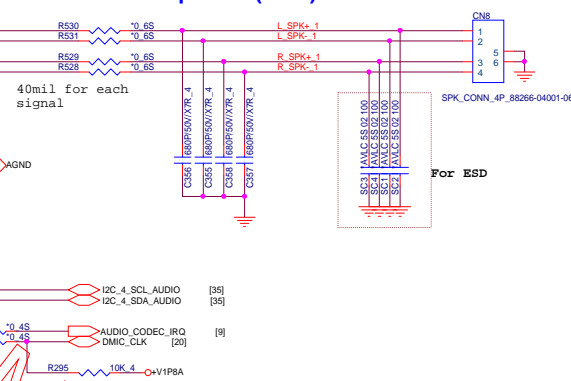
Codec (ADO)



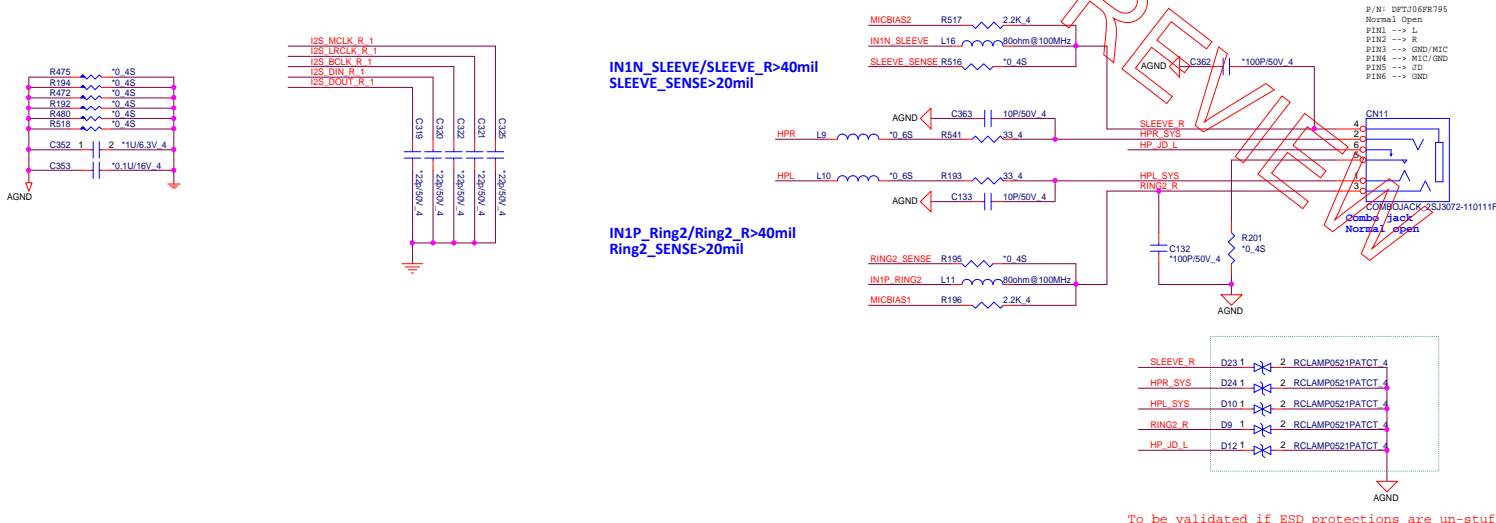
Codec PWR 5V (ADO)



Internal Speaker (ADO)



Combo Jack (ADO)

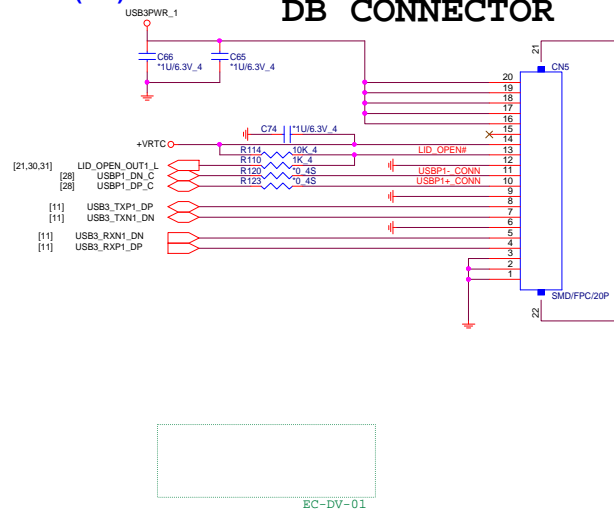


To be validated if ESD protections are un-stuffed

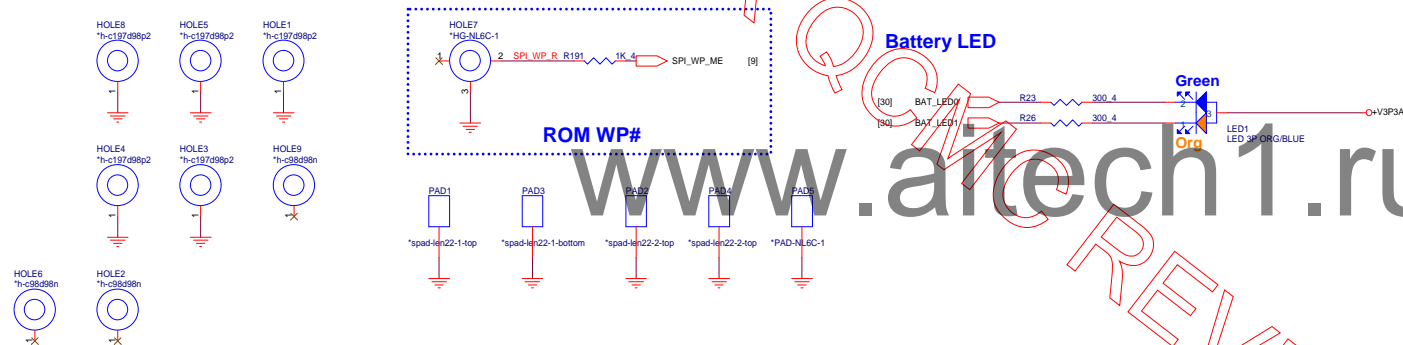
TPM



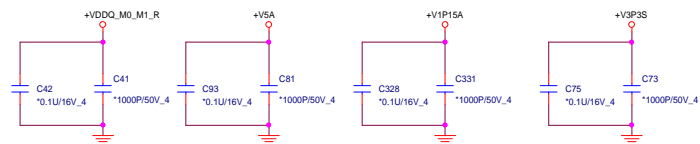
DB CONNECTOR



Holes(OTH) MOUNTING HOLES

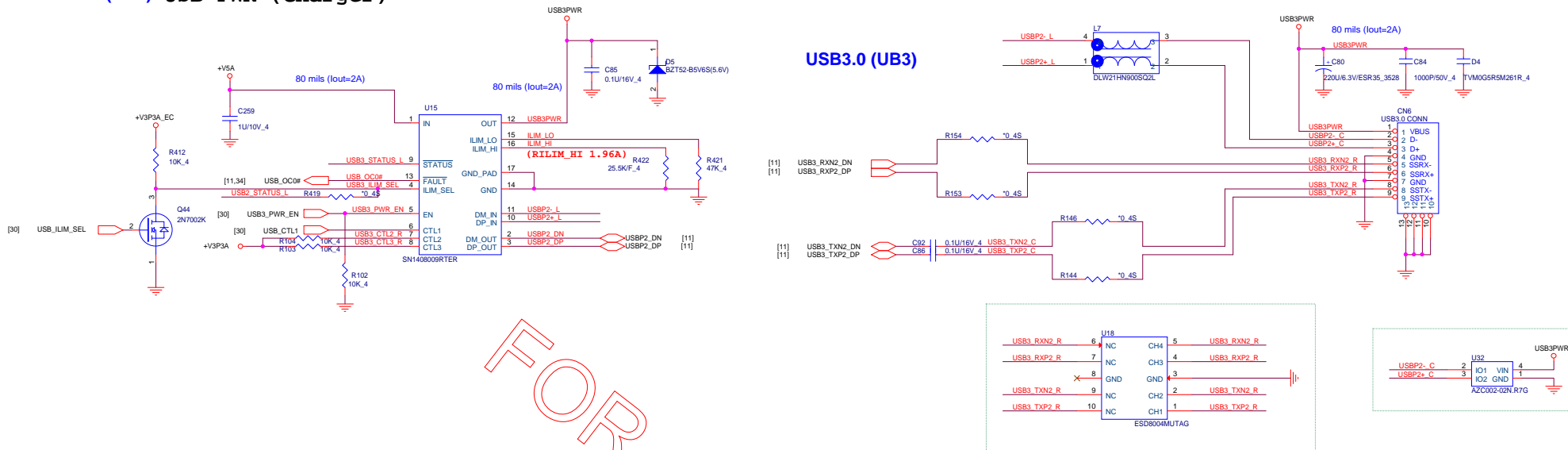


EMI caps



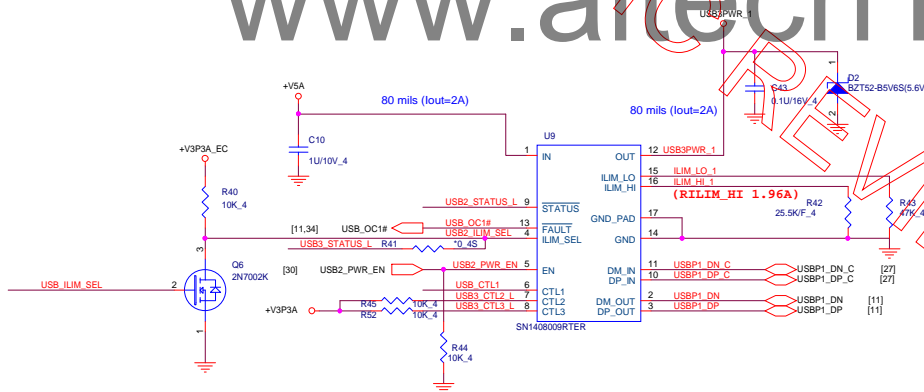
RF caps

USB3.0 (UB3) USB PWR (Charger)



USB PWR(Charger)

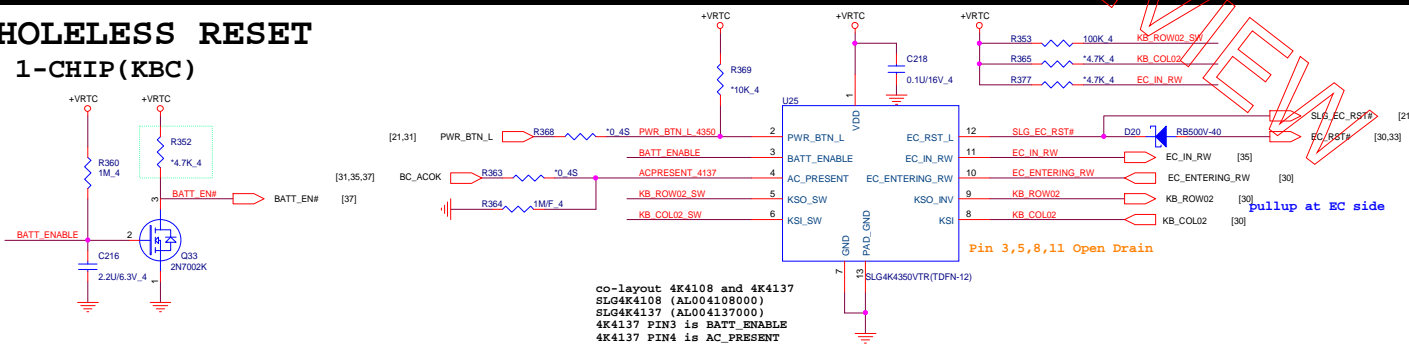
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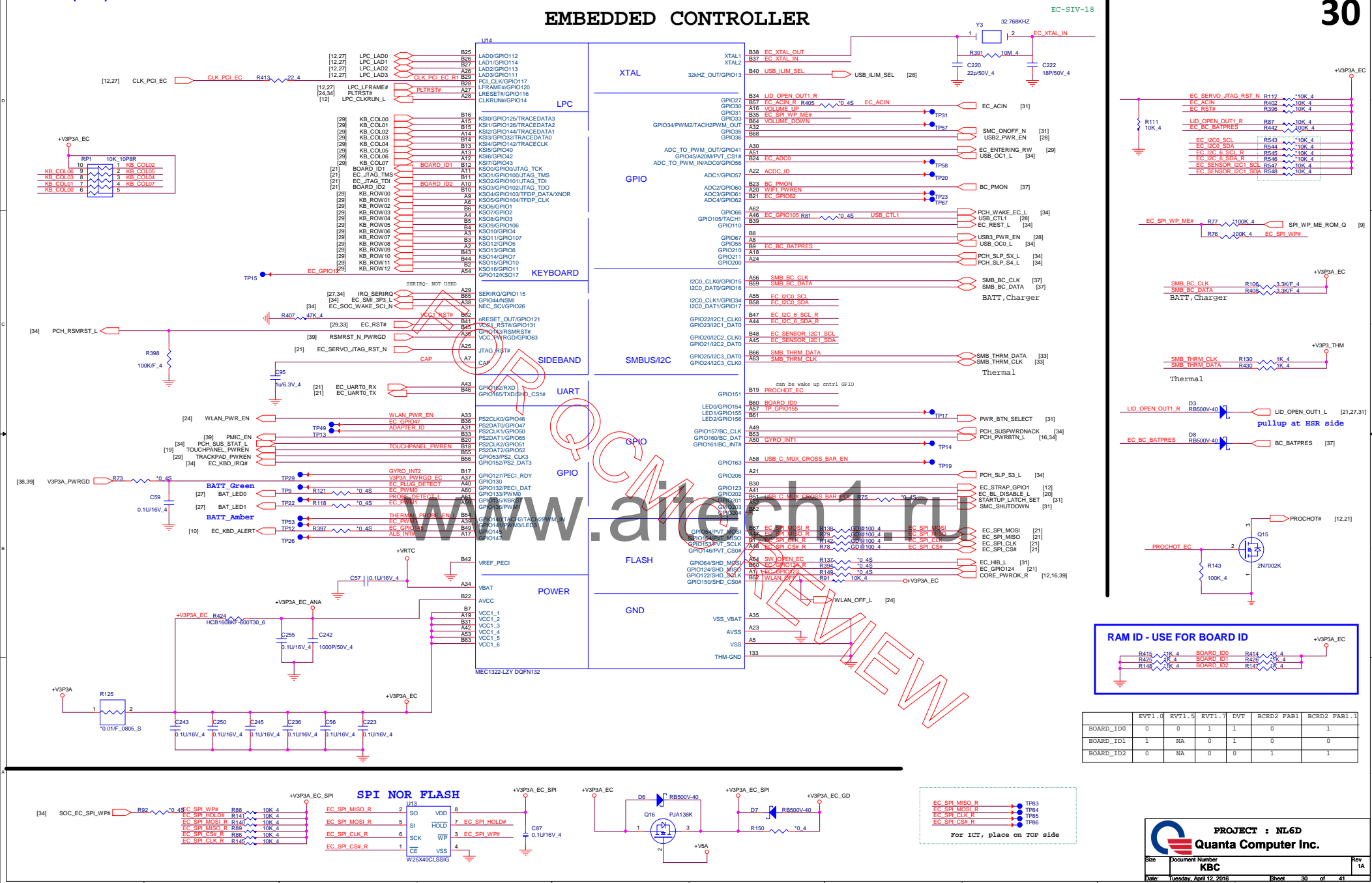


HOLELESS RESET

1-CHIP (KBC)



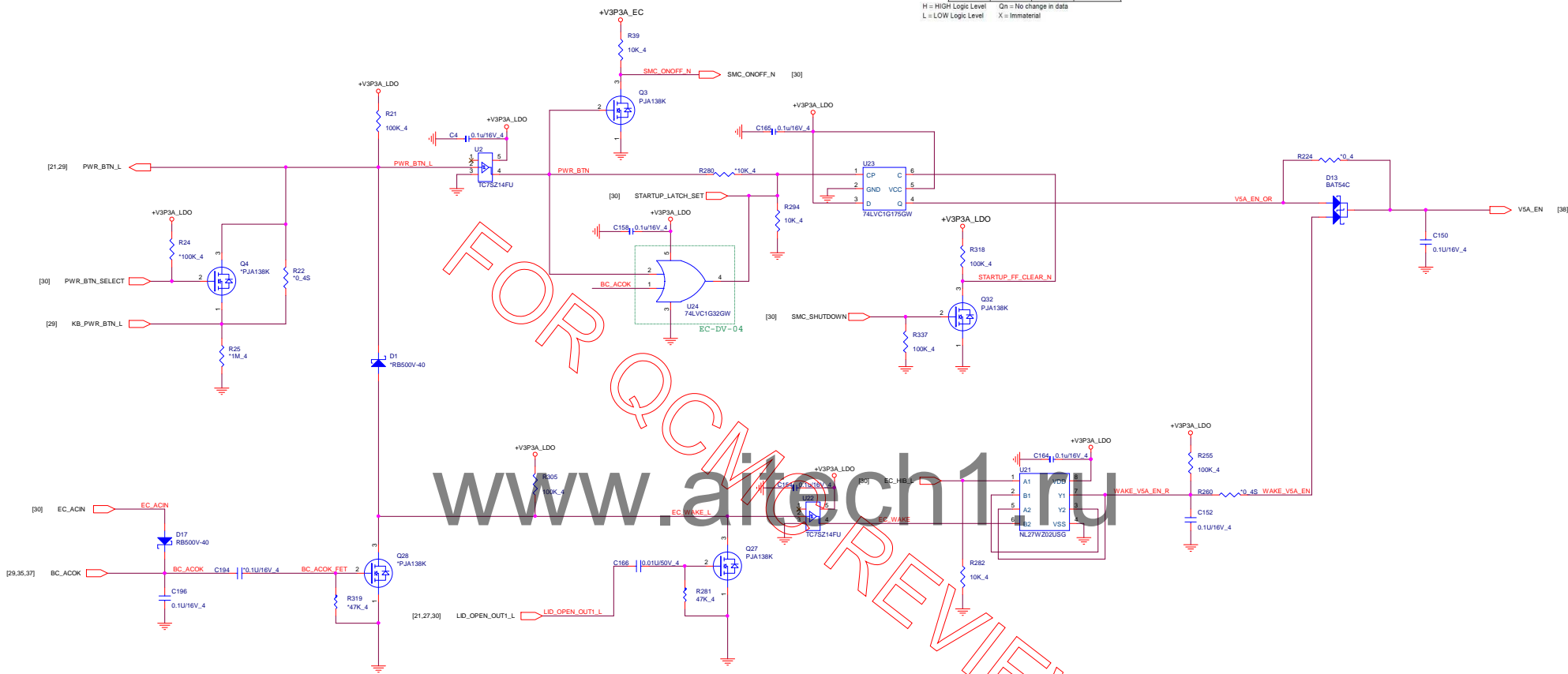
EMBEDDED CONTROLLER



Function Table

Inputs				Output
CP	D	C	Q	
	L	H	L	L
	H	H	H	H
	X	H	L	Qn
	X	X	L	L

H = HIGH Logic Level
L = LOW Logic Level
Qn = No change in data
X = Immaterial



EC HIB WAKE SOURCES

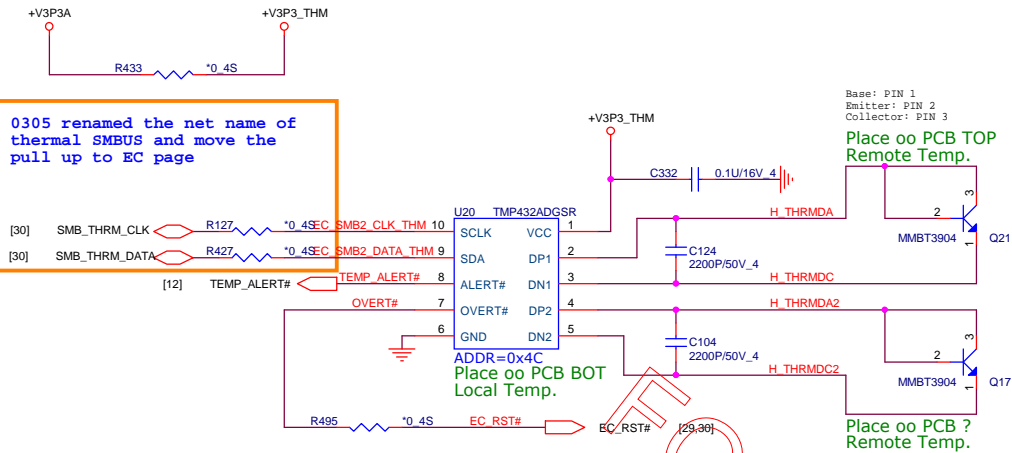
Removed (2015/03/30)

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Thermal (THM)

THERMAL SENSOR



ACCELEROMETER

G-Sensor (ACS)

Removed (2015/03/27)

Touch screen(TSN)


Touch screen(TSN)

Removed (2015/03/27)

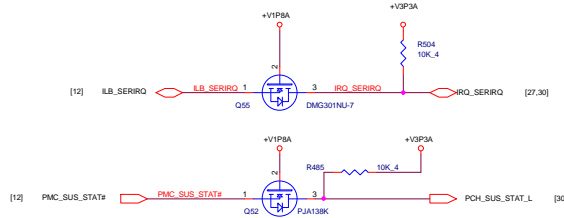
Removed (2015/03/27)

LED board(UIF)

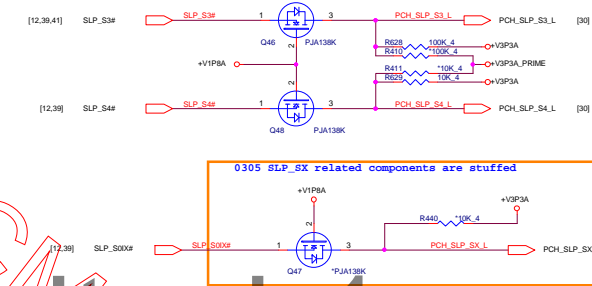
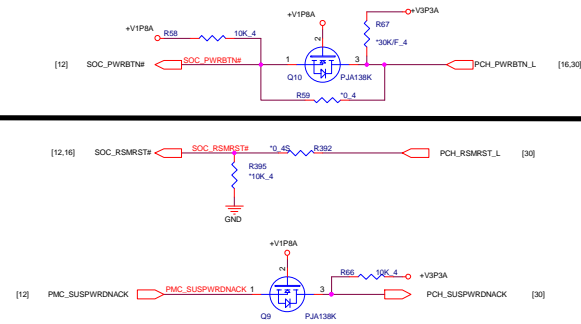
Removed (2015/03/27)

		PROJECT : NL6D	
		Quanta Computer Inc.	
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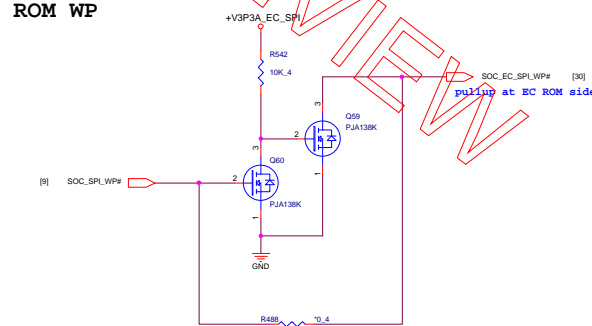
PWRON SEQUENCE



PWRON SEQUENCE

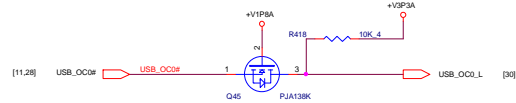


ROM WP

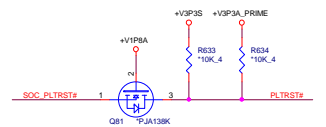
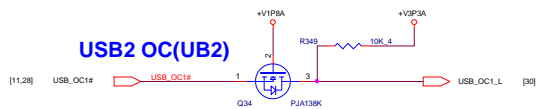


USB OC

USB3 OC(UB3)

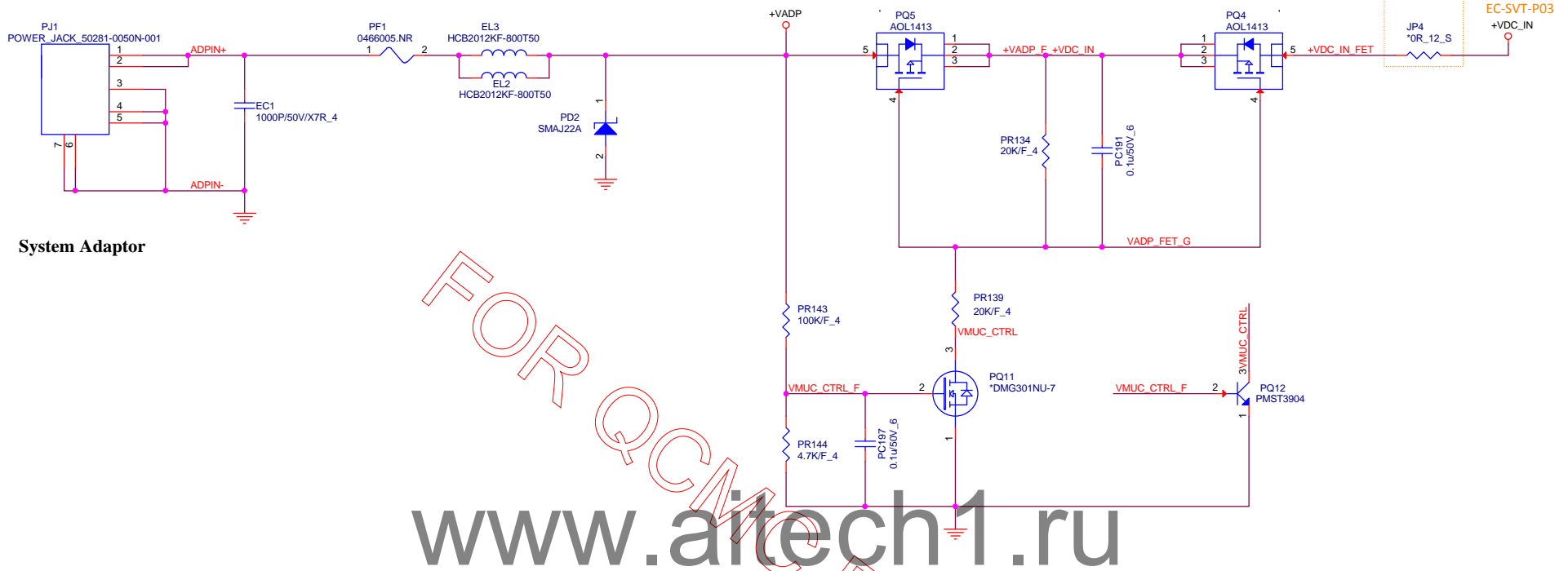


USB2 OC(UB2)



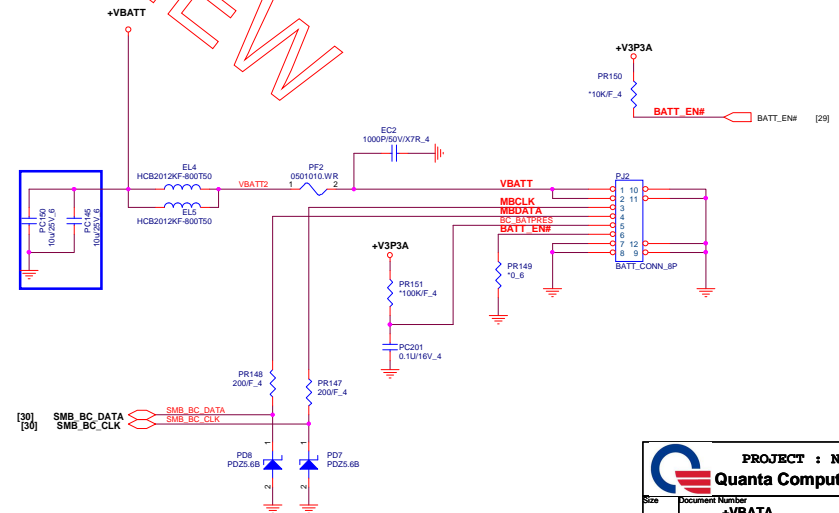
DC JACK

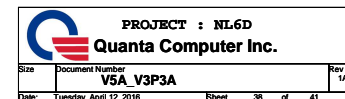
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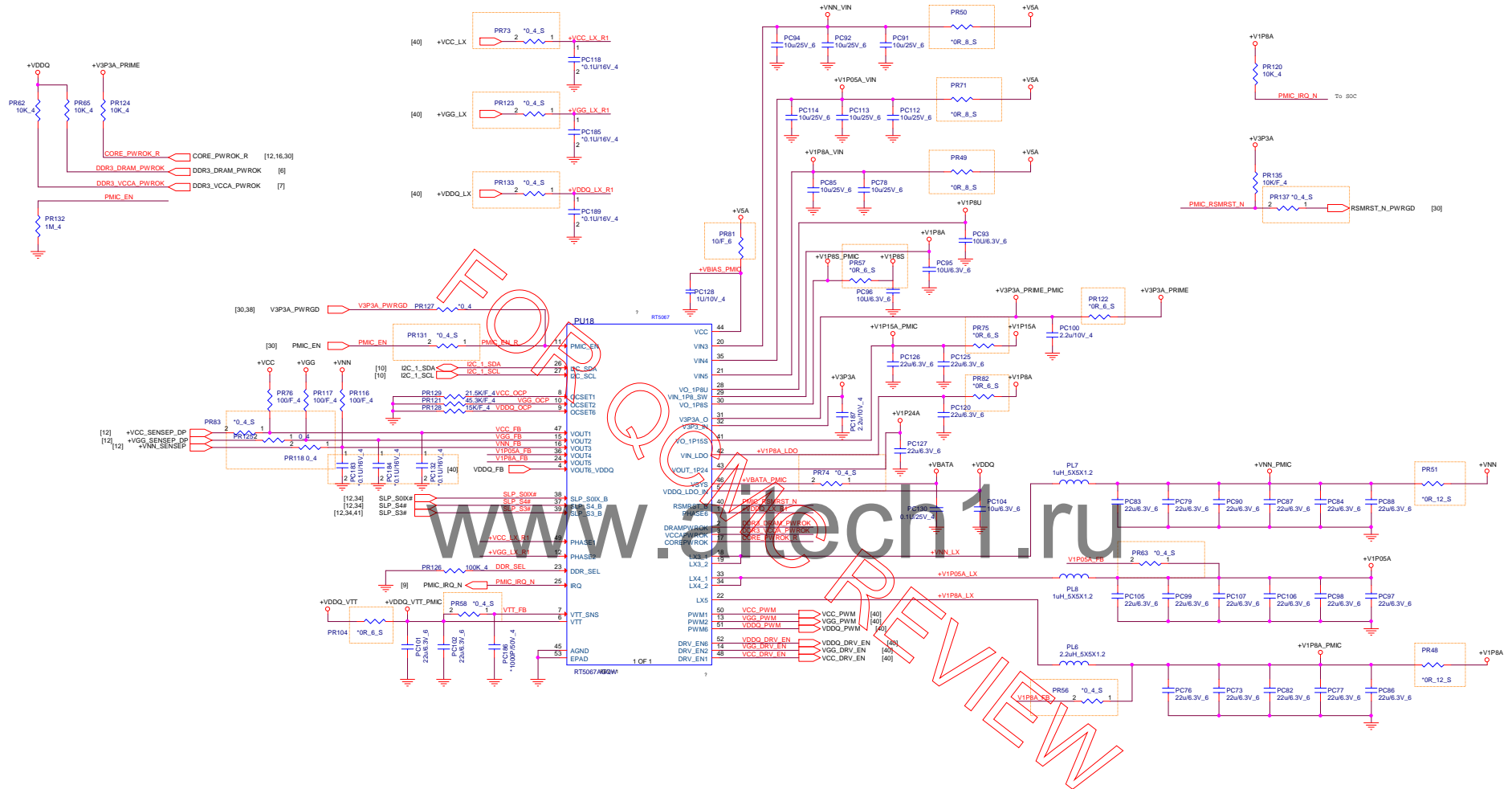




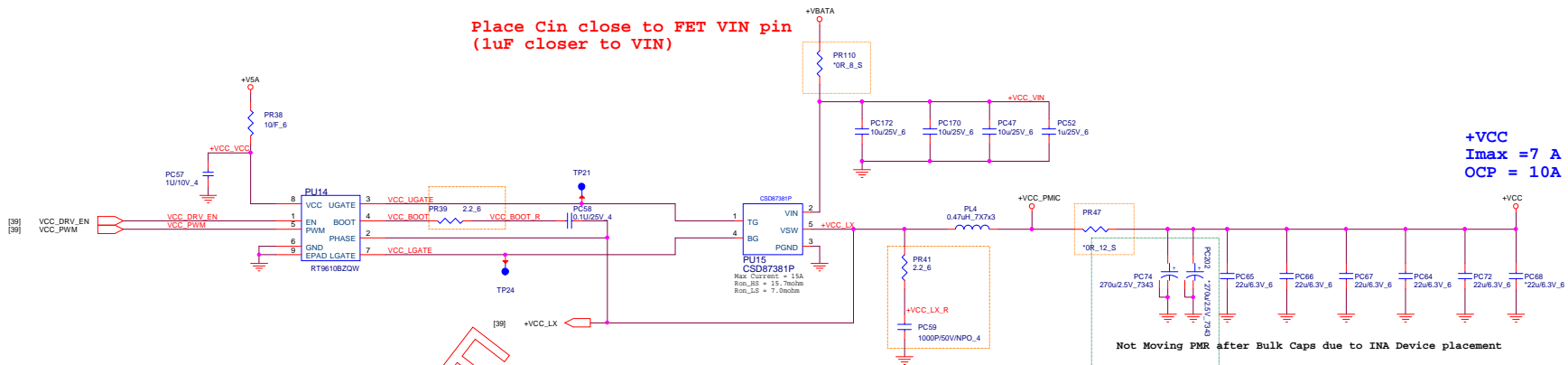
~~BATTERY CONNECTOR~~



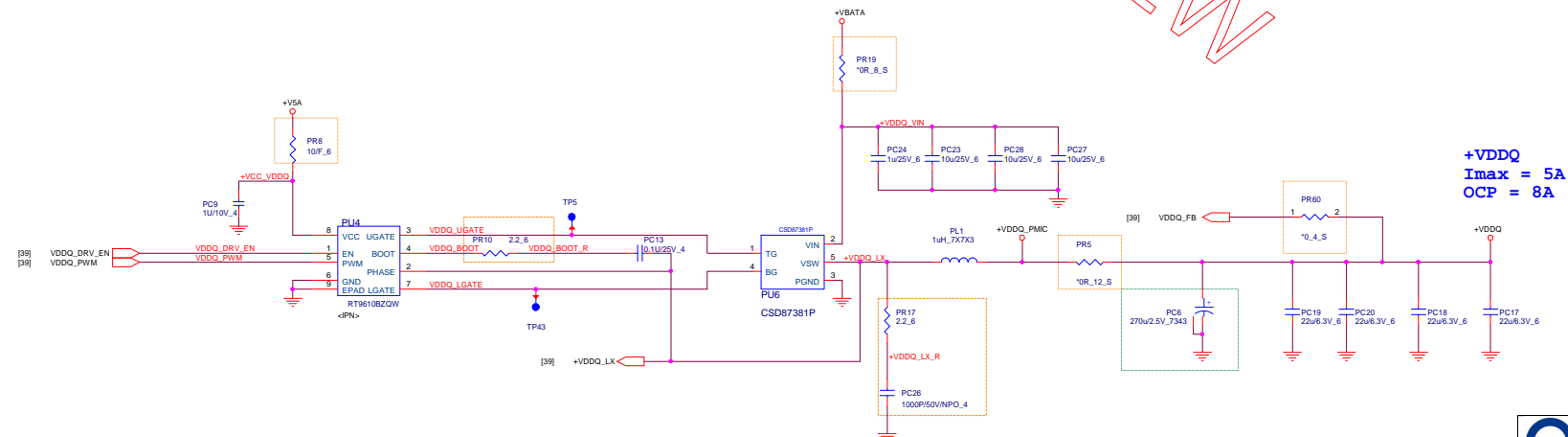
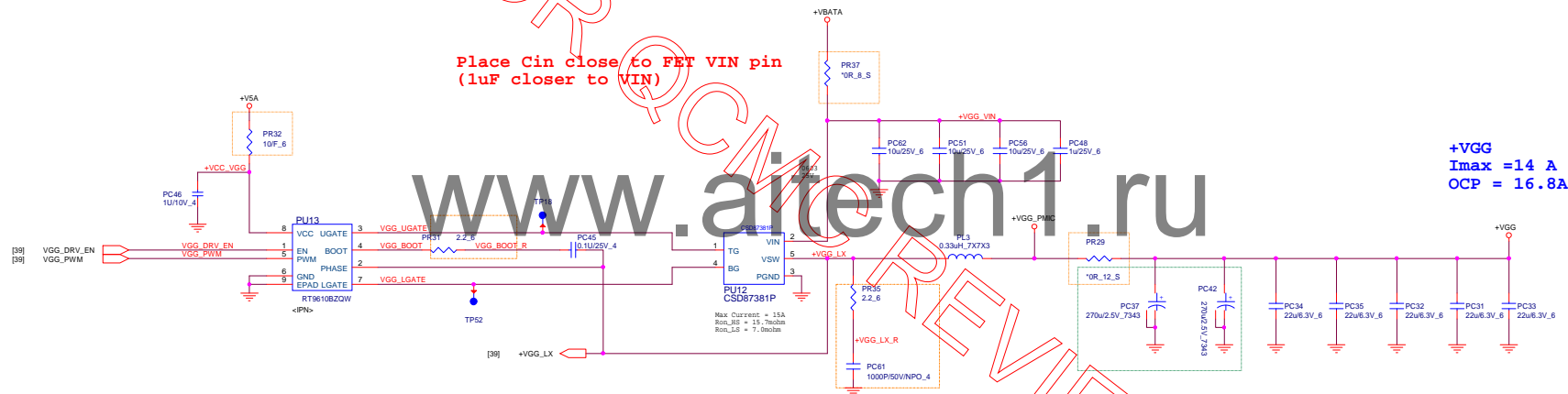




Place Cin close to FET VIN pin
(1uF closer to VIN)



Place Cin close to FET VIN pin
(1uF closer to VIN)



CHECK SLEW RATE



Notes:
Imax: 4A
Rise time: 1ms

Notes:
Imax: 100 mA
Rise time: 150 uSec

[illegible]